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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	ATTORNEY DOCKET NO. CONFIRMATION NO.	
10/647,696	08/25/2003	Mohan Kirloskar	50626.54 2471		
75	90 06/21/2004		EXAMINER		
KEATING & BENNETT LLP			BEREZNY, NEMA O		
Suite 312 10400 Eaton Place		ART UNIT	PAPER NUMBER		
Fairfax, VA 2			2813		
			DATE MAILED: 06/21/200	DATE MAILED: 06/21/2004	

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)				
	10/647,696	KIRLOSKAR ET AL.				
Office Action Summary	Examin r	Art Unit				
	Nema O Berezny	2813				
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply						
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.  - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.  - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.  - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).						
Status						
1) Responsive to communication(s) filed on						
2a) This action is <b>FINAL</b> . 2b) ☐ This	action is non-final.					
3) Since this application is in condition for allowa	3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is					
closed in accordance with the practice under E	Ex parte Quayle, 1935 C.D. 11, 45	i3 O.G. 213.				
Disposition of Claims						
4) Claim(s) 1-30 is/are pending in the application						
4a) Of the above claim(s) <u>25-30</u> is/are withdrawn from consideration.						
5) Claim(s) is/are allowed.						
6)⊠ Claim(s) <u>1-24</u> is/are rejected.						
7) Claim(s) is/are objected to.						
8) Claim(s) are subject to restriction and/or election requirement.						
Application Papers	Application Papers					
9)☐ The specification is objected to by the Examiner.						
10)⊠ The drawing(s) filed on <u>25 August 2003</u> is/are: a)⊠ accepted or b)□ objected to by the Examiner.						
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).						
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).						
11) The oath or declaration is objected to by the Ex	caminer. Note the attached Office	Action or form PTO-152.				
Priority under 35 U.S.C. § 119						
12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of:						
1. Certified copies of the priority documents have been received.						
2. Certified copies of the priority documents have been received in Application No						
3. Copies of the certified copies of the priority documents have been received in this National Stage						
application from the International Bureau (PCT Rule 17.2(a)).						
* See the attached detailed Office action for a list of the certified copies not received.						
Attachment(s)						
1) Notice of References Cited (PTO-892)  4) Interview Summary (PTO-413)						
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date  5) Notice of Informal Patent Application (PTO-152)					
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>08252003, 03172004</u> .	6) Other:					

#### **DETAILED ACTION**

### Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

- Claims 1-24, drawn to a method of making a semiconductor device, classified in class 438, subclass 122.
- Claims 25-30, drawn to a semiconductor device, classified in class 257, subclass 712.

The inventions are distinct, each from the other because of the following reasons:

Inventions I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case, the product as claimed can be made by another and materially different process, for instance, the claimed device could be made from individual substrates rather than processed and then singulated from a larger substrate or wafer.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

During a telephone conversation with Chris Bennett on 6-9-04 a provisional election was made without traverse to prosecute the invention of Group I, claims 1-24. Affirmation of this election must be made by applicant in replying to this Office action. Claims 25-30 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

#### Information Disclosure Statement

The IDS submitted and filed on 1-26-04 has not been considered because it contains an incorrect serial number (10/643,961). If Applicant intended for said IDS to be submitted as part of instant application, Applicant needs to resubmit said IDS with the proper serial number.

## Claim Objections

Claim 6 is objected to because of the following informalities: in line 1 after "wherein", delete "said mounting". Appropriate correction is required.

## Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 13 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Said claim 13 states that collapsible spacers are disposed between and in contact with said heat spreader during molding. Two objects (said heat spreader and another object) are required for said spacers to be disposed there between. Correction is required.

Claim 24 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Said claim 24 states that collapsible spacer arrays are disposed <u>between</u> and in contact with said heat spreader during molding. Two objects (said heat spreader and another object) are required for said spacers to be disposed there between. Correction is required.

## Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 4-7, and 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Atwood et al. (6,656,770) in view of Tonti et al. (5,773,362). Atwood discloses a process for manufacturing an integrated circuit package or a plurality of integrated circuit packages comprising: mounting a semiconductor die or dice (Fig.1 el.12), to a first surface of a substrate or substrate array (el.10) such that bumps (el.11) on said semiconductor die or dice are electrically connected to conductive traces (inherent) of said substrate; mounting a collapsible spacer or spacer array (el.18) to at least one of a heat spreader or heat spreader array (el.14), said semiconductor die and said substrate or substrate array (col.11 lines 47-64); fixing said heat spreader to at least one of said first surface of said substrate and said semiconductor die such that said at least one collapsible spacer is disposed therebetween (Fig.1); forming a ball grid array or a plurality of ball grid arrays (no #) on a second surface of said substrate, bumps of said ball grid array being electrically connected to said conductive traces (inherent). However, Atwood does not disclose singulating said package or packages. Atwood would look to one such as Tonti for more efficient IC fabrication because Tonti discloses singulating said integrated circuit package (col.1 lines 43-64). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the

invention to use the singulating of Tonti with the process of Atwood in order to mass fabricate a large number of packages in a single process step, thereby saving time and costs [claim 1].

Based upon the rejection of claim 1 above, Atwood also discloses wherein fixing said heat spreader comprises reflowing of the at least one collapsible spacer (col.11 lines 24-30) [claim 4]; wherein said mounting a semiconductor die comprises mounting said semiconductor die in a flip-chip orientation, to said substrate (Fig.1) [claim 5]; wherein said mounting said semiconductor die comprises solder reflowing thereby connecting said bumps of said semiconductor die in said flip-chip orientation to said conductive traces of said substrate (col.9 lines 41-42) [claim 6]; wherein said mounting further comprises underfilling said semiconductor die (Fig.3) [claim 7]; wherein said mounting at least one collapsible spacer comprises mounting said at least one collapsible spacer to said substrate (Fig.1; col.9 lines 53-54) [claim 10]; wherein said mounting at least one collapsible spacer comprises mounting said at least one collapsible spacer to said heat spreader (Fig.1) [claim 11]; and wherein said at least one collapsible spacer comprises a plurality of collapsible spacers, and mounting said at least one collapsible spacer comprises mounting one of said plurality of collapsible spacers to said semiconductor die and mounting at least another of said collapsible spacers to said substrate (Fig.1) [claim 12].

Claims 2, 8-9, and 13-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Atwood in view of Tonti as applied to claims 1 and 12 above, and

further in view of Sono et al. (5,444,025). Atwood in view of Tonti do not disclose molding said die, said substrate, said collapsible spacer, and said heat spreader in a molding compound. Atwood and Tonti would look to one such as Sono for device protection because Sono discloses wherein fixing said heat spreader comprises: placing one of said heat spreader and said substrate in a mold cavity (Fig.3B); releasably clamping the other of said heat spreader and said substrate to a die of said mold cavity, such that said collapsible spacer is disposed between said heat spreader and said substrate (col.4 lines 16-20); and molding a molding compound in the mold, thereby molding the semiconductor die, the substrate, said at least one collapsible spacer, and said heat spreader into the molding compound to provide a molded package (Fig.6 el.7). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the molding of Sono with the process of Atwood in view of Tonti in order to protect the device from moisture, and chemical and mechanical stress; and to provide highly accurate placement of the heatsink (col.4 lines 25-30) [claims 2, 15]. Atwood and Tonti would look to one such as Sono for accurate mold placement because Sono discloses wherein said placing one of said heat spreader and said substrate in a mold cavity comprises placing said heat spreader in said mold cavity such that said heat spreader rests on a lower die of said mold and said releasably clamping comprises releasably clamping said substrate to an upper die of said mold (Figs.3A-3E). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the molding of Sono with the process of Atwood in view of Tonti in order to accurately place and secure each device element in

the molds from movement; wherein the top and bottom dies are only relative to each other [claims 8, 9, 19, 20].

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Based upon the rejection of claims 1-2, 8-9, and 12 above, Atwood discloses wherein said at least another of said collapsible spacers is disposed in contact with said heat spreader during molding (Fig.1) [claims 13, 14].

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Atwood in view of Tonti as applied to claim 1 above, and further in view of Huang et al. (2002/0180035). Atwood in view of Tonti do not disclose thermally curing said collapsible spacer. Atwood and Tonti would look to one such as Huang for thermal conductivity because Huang discloses wherein fixing said heat spreader comprises thermal curing of the at least one collapsible spacer (Fig.1 el.26; p.3 para.35). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the thermal curing of Huang with the process of Atwood in view of Tonti in order to provide a spacer between the chip and heat spreader that is electrically isolated but still thermally conductive.

Based upon the rejection of claim 15 above, wherein said mounting semiconductor dice comprises mounting said semiconductor dice in a flip-chip orientation, to said substrate array (Fig.1) [claim 16]; wherein said mounting said semiconductor dice comprises solder reflowing thereby connecting said bumps of said semiconductor dice in said flip-chip orientation to said conductive traces of said substrate array (col.9 lines 41-42) [claim 17]; wherein said mounting further comprises

underfilling said semiconductor dice (Fig.3) [claim 18]; wherein said mounting said spacer array comprises mounting said collapsible spacer array to said substrate array (Fig.1; col.9 lines 53-54) [claim 21]; wherein said mounting said collapsible spacer array comprises mounting said collapsible spacer array to said heat spreader array (Fig.1) [claim 22]; wherein mounting said collapsible spacer array further comprises mounting a corresponding collapsible spacer of said collapsible spacer array to each of said plurality of semiconductor dice (Fig.1) [claim 23]; and wherein said collapsible spacer array is disposed between and in contact with said heat spreader during molding (Fig.1) [claim 24].

#### Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nema O Berezny whose telephone number is (571) 272-1686. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Art Unit: 2813

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NB

Chandra Chaudhari Primary Examiner

Chandra Gaudhari